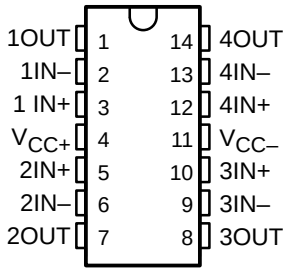
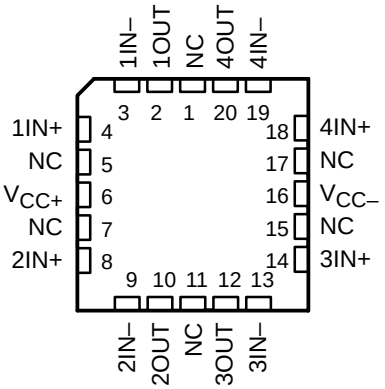
- **μA741 Operating Characteristics**
- **Low Supply-Current Drain . . . 0.6 mA Typ (per amplifier)**
- **Low Input Offset Voltage**
- **Low Input Offset Current**
- **Class AB Output Stage**
- **Input/Output Overload Protection**
- **Designed to Be Interchangeable With Industry Standard LM148, LM248, and LM348**

LM148 . . . J PACKAGE
LM248 . . . D OR N PACKAGE
LM348 . . . D, N, OR NS PACKAGE
(TOP VIEW)



LM148 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

The LM148, LM248, and LM348 are quadruple, independent, high-gain, internally compensated operational amplifiers designed to have operating characteristics similar to the μA741. These amplifiers exhibit low supply-current drain and input bias and offset currents that are much less than those of the μA741.

ORDERING INFORMATION

T_A	V_{IO}max AT 25°C	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	6 mV	PDIP (N)	Tube of 25	LM348N	LM348N
		SOIC (D)	Tube of 50	LM348D	LM348
			Reel of 2500	LM348DR	
		SOP (NS)	Reel of 2000	LM348NSR	LM348
–25°C to 85°C	6 mV	PDIP (N)	Tube of 25	LM248N	LM248N
		SOIC (D)	Tube of 50	LM248D	LM248
			Reel of 2500	LM248DR	
–55°C to 125°C	5 mV	CDIP (J)	Tube of 25	LM148J	LM148J
		LCCC (FK)	Tube of 50	LM148FK	LM148FK

† Package drawings, standard packing quantities, thermal data, symboliztion, and PCB design guidelines are available at www.ti.com/sc/package.

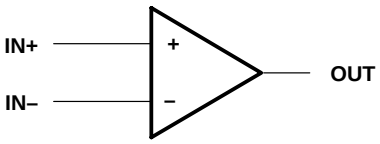
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2002, Texas Instruments Incorporated

On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

symbol (each amplifier)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC+} (see Note 1): LM148 . . . . . 22 V
LM248, LM348 . . . . . 18 V
Supply voltage, $V_{CC–}$ (see Note 1): LM148 . . . . . –22 V
LM248, LM348 . . . . . –18 V
Differential input voltage, V_{ID} (see Note 2): LM148 . . . . . 44 V
LM248, LM348 . . . . . 36 V
Input voltage, V_I (either input, see Notes 1 and 3): LM148 . . . . . –22 V
LM248, LM348 . . . . . –18 V
Duration of output short circuit (see Note 4) . . . . . Unlimited
Operating virtual junction temperature, T_J . . . . . 150°C
Package thermal impedance, θ_{JA} (see Notes 5 and 6): D package . . . . . 86°C/W
N package . . . . . 80°C/W
NS package . . . . . 76°C/W
Package thermal impedance, θ_{JC} (see Notes 7 and 8): FK package . . . . . 5.61°C/W
J package . . . . . 15.05°C/W
Case temperature for 60 seconds: FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: D, N, or NS package . . . . . 260°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and $V_{CC–}$.
2. Differential voltages are at IN+ with respect to IN–.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or the value specified in the table, whichever is less.
4. The output may be shorted to ground or either power supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.
5. Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperautre is $P_D = (T_J(max) – T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
6. The package thermal impedance is calculated in accordance with JESD 51-7.
7. Maximum power dissipation is a function of $T_J(max)$, θ_{JC}, and T_C. The maximum allowable power dissipation at any allowable ambient temperautre is $P_D = (T_J(max) – T_C)/\theta_{JC}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
8. The package thermal impedance is calculated in accordance with MIL-STD-883.

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{CC+}	4	18	V
Supply voltage, $V_{CC–}$	–4	–18	V

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			LM148			LM248			LM348			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0		25°C		1	5		1	6		1	6	mV
				Full range			6			7.5			7.5	
I_{IO}	Input offset current	V_O = 0		25°C		4	25		4	50		4	50	nA
				Full range			75			125			100	
I_{IB}	Input bias current	V_O = 0		25°C		30	100		30	200		30	200	nA
				Full range			325			500			400	
V_{ICR}	Common-mode input voltage range			Full range	±12			±12			±12			V
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ		25°C	±12	±13		±12	±13		±12	±13		V
		R_L ≥ 10 kΩ		Full range	±12			±12			±12			
		R_L = 2 kΩ		25°C	±10	±12		±10	±12		±10	±12		
		R_L ≥ 2 kΩ		Full range	±10			±10			±10			
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V, R_L = ≥ 2 kΩ		25°C	50	160		25	160		25	160		V/mV
				Full range	25			15			15			
r_i	Input resistance‡			25°C	0.8	2.5		0.8	2.5		0.8	2.5		MΩ
B_1	Unity-gain bandwidth	A_{VD} = 1		25°C		1			1			1		MHz
ϕ_m	Phase margin	A_{VD} = 1		25°C		60°			60°			60°		
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, V_O = 0		25°C	70	90		70	90		70	90		dB
				Full range	70			70			70			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±9 V to ±15 V, V_O = 0		25°C	77	96		77	96		77	96		dB
				Full range	77			77			77			
I_{OS}	Short-circuit output current			25°C		±25			±25			±25		mA
I_{CC}	Supply current (four amplifiers)	No load	V_O = 0	25°C					2.4	4.5		2.4	4.5	mA
			V_O = V_{OM}			2.4	3.6							
V_{O1}/V_{O2}	Crosstalk attenuation	f = 1 Hz to 20 kHz		25°C		120			120			120		dB

† All characteristics are measured under open-loop conditions with zero common-mode input voltage, unless otherwise specified. Full range for T_A is –55°C to 125°C for LM148, –25°C to 85°C for LM248, and 0°C to 70°C for LM348.

‡ This parameter is not production tested.

operating characteristics, $V_{CC\pm}$ = ±15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 2 kΩ, C_L = 100 pF, See Figure 1		0.5		V/μs

PARAMETER MEASUREMENT INFORMATION

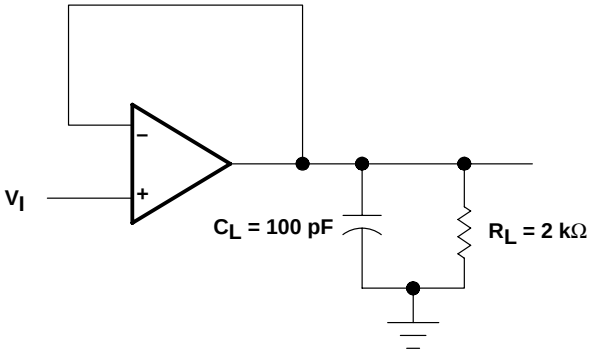


Figure 1. Unity-Gain Amplifier

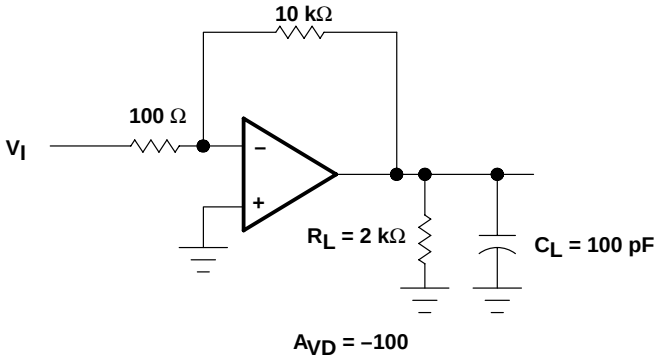


Figure 2. Inverting Amplifier

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM148 MW8	ACTIVE	WAFERSALE	YS	0	1	RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125		Samples
LM148FKB	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	LM148FKB	Samples
LM148J	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	LM148J	Samples
LM148JB	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	LM148JB	Samples
LM248D	LIFEBUY	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM248	
LM248DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM248	Samples
LM248N	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-25 to 85	LM248N	Samples
LM348D	LIFEBUY	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM348	
LM348DG4	LIFEBUY	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM348	
LM348DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM348	Samples
LM348DRE4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM348	Samples
LM348DRG4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM348	Samples
LM348N	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	LM348N	Samples
LM348NSR	LIFEBUY	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM348	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

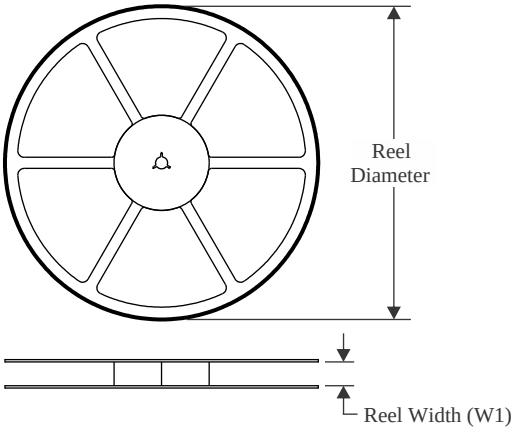
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

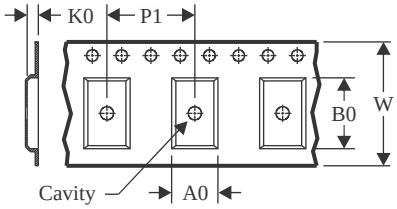
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

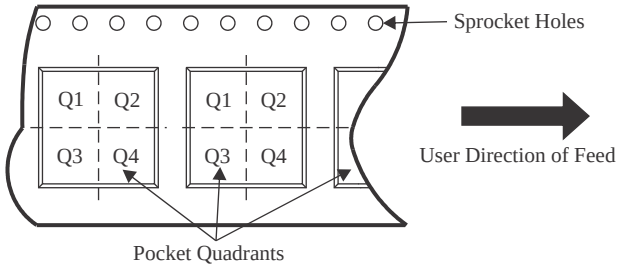


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

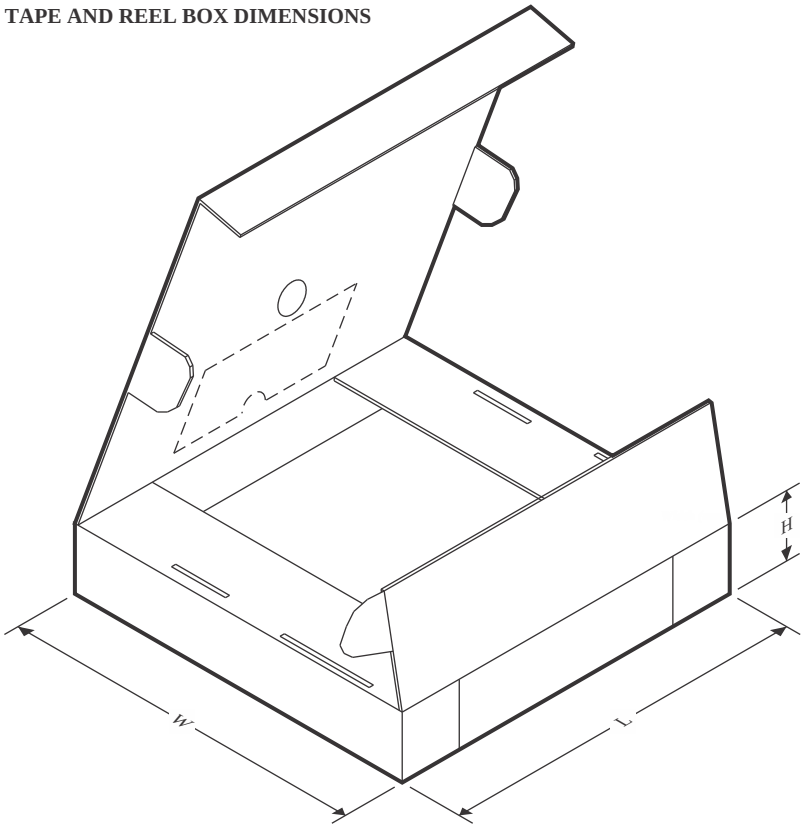
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM248DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM348DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM348NSR	SO	NS	14	2000	330.0	16.4	8.45	10.55	2.5	12.0	16.2	Q1

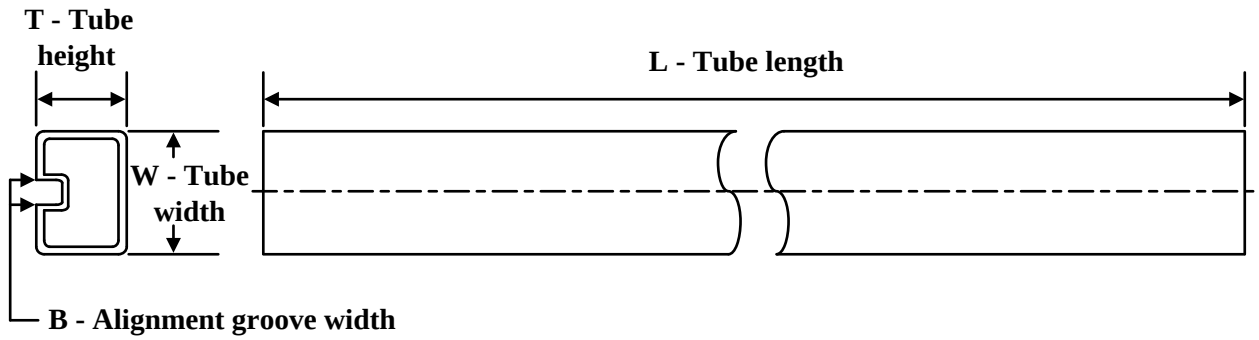
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM248DR	SOIC	D	14	2500	356.0	356.0	35.0
LM348DR	SOIC	D	14	2500	333.2	345.9	28.6
LM348NSR	SO	NS	14	2000	356.0	356.0	35.0

TUBE



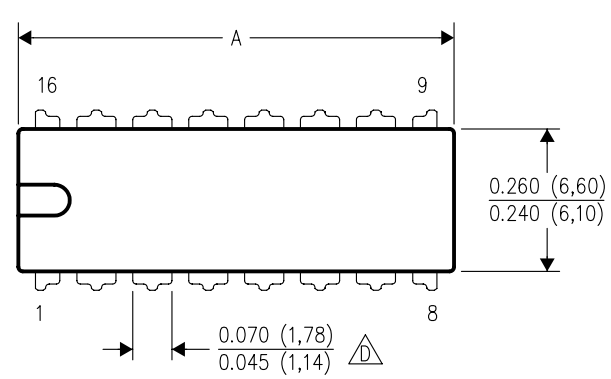
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM148FKB	FK	LCCC	20	55	506.98	12.06	2030	NA
LM248D	D	SOIC	14	50	506.6	8	3940	4.32
LM248N	N	PDIP	14	25	506	13.97	11230	4.32
LM348D	D	SOIC	14	50	506.6	8	3940	4.32
LM348D	D	SOIC	14	50	507	8	3940	4.32
LM348DG4	D	SOIC	14	50	507	8	3940	4.32
LM348DG4	D	SOIC	14	50	506.6	8	3940	4.32
LM348N	N	PDIP	14	25	506	13.97	11230	4.32

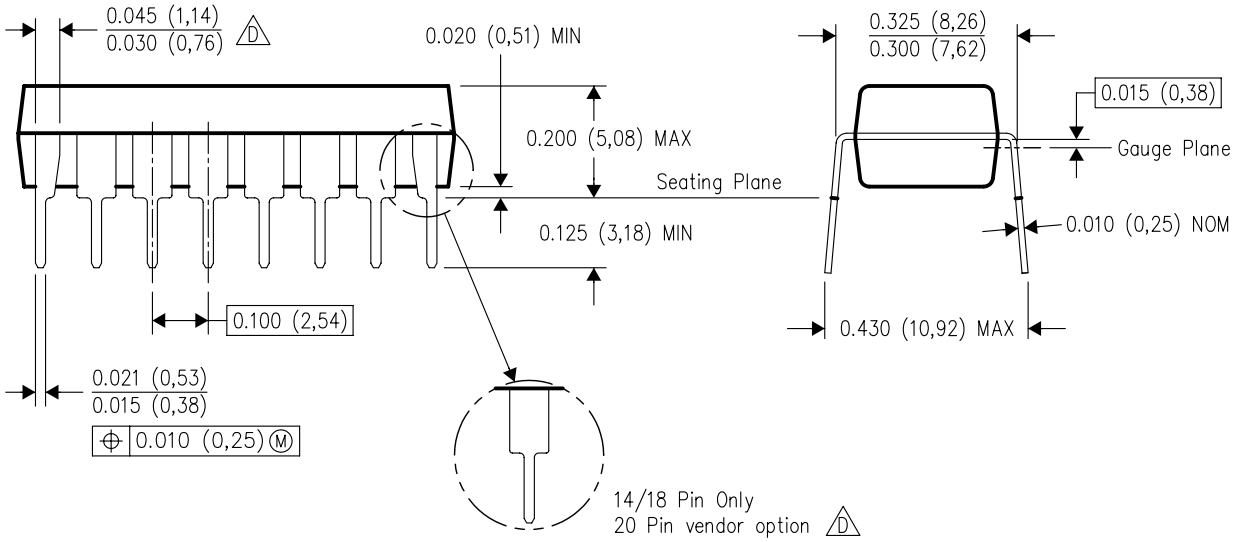
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



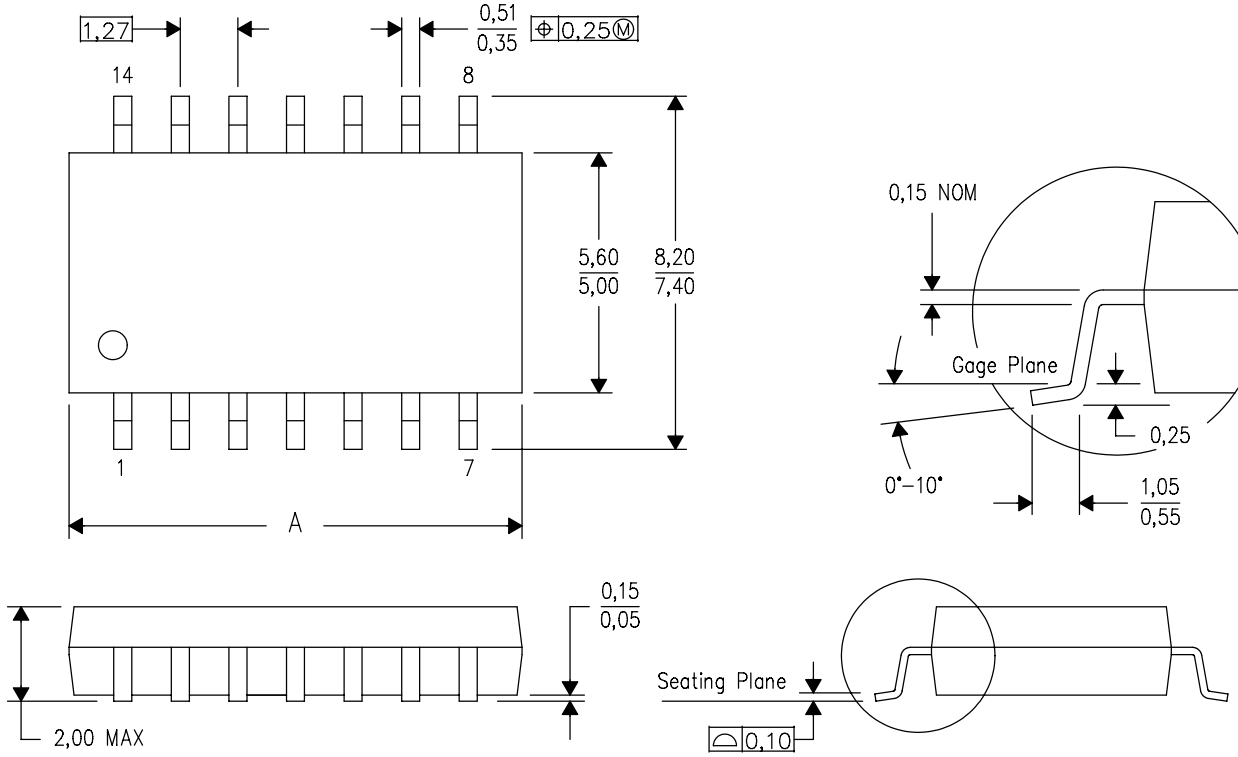
4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

GENERIC PACKAGE VIEW

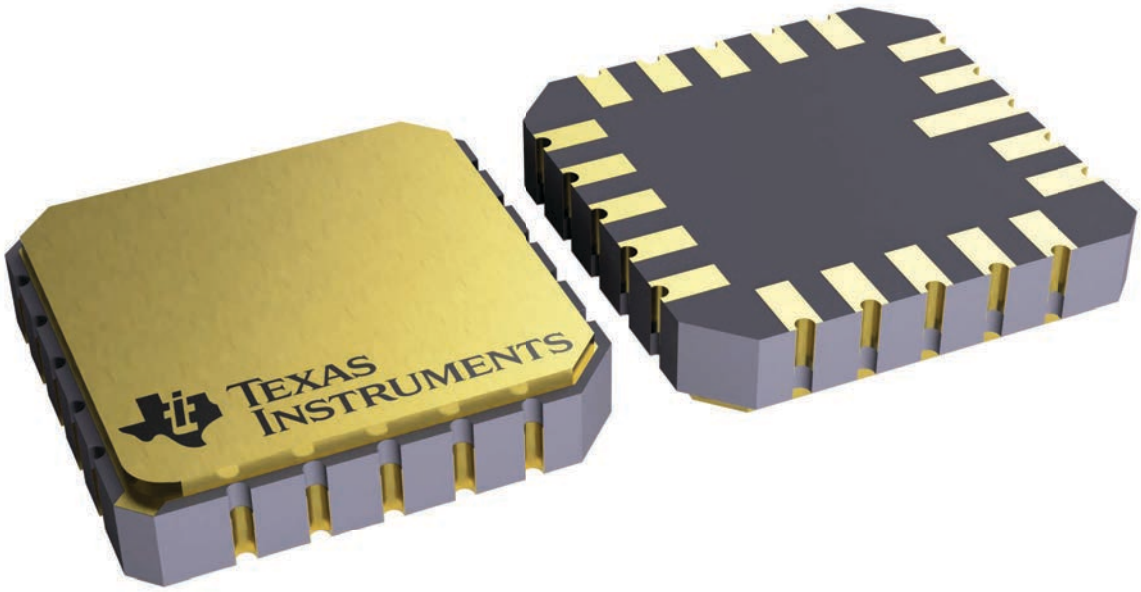
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

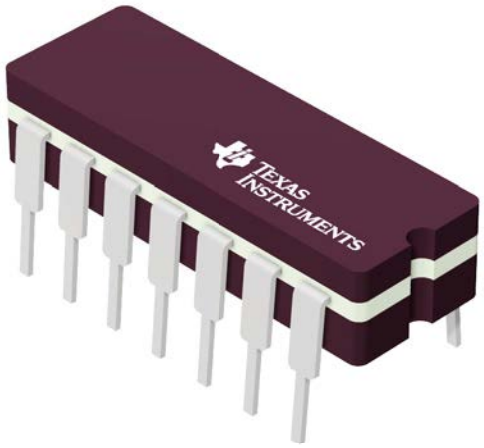


4229370VA\

GENERIC PACKAGE VIEW

J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

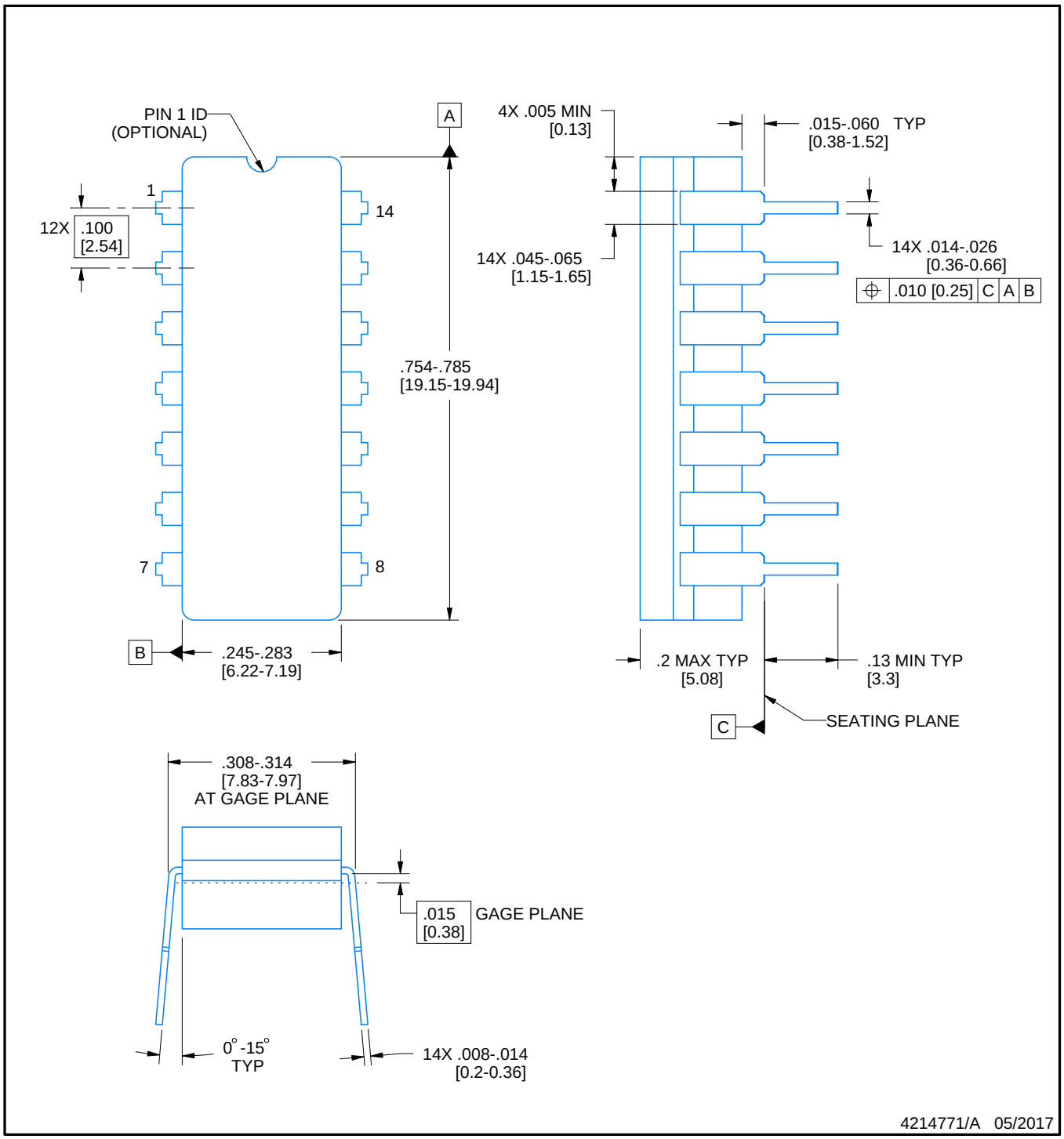


PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



NOTES:

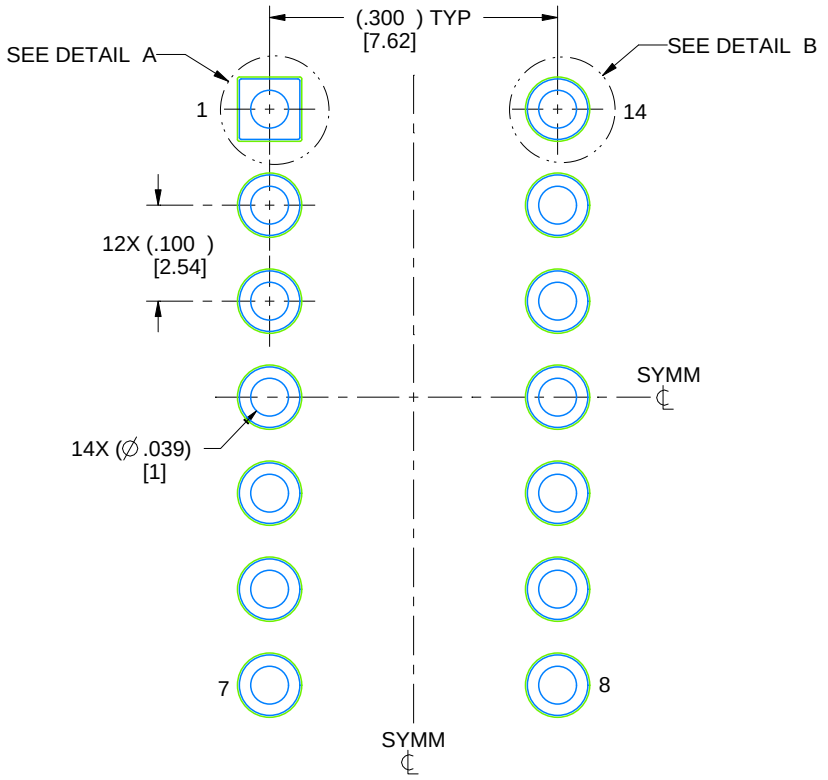
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

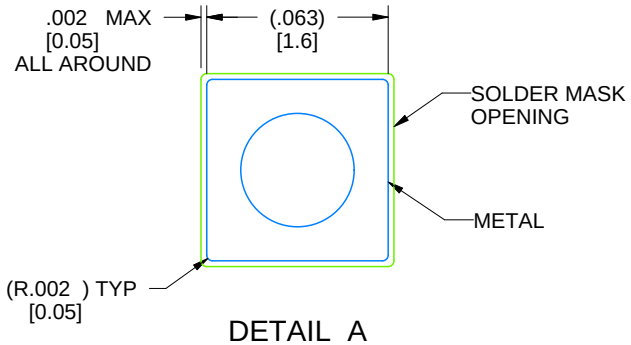
J0014A

CDIP - 5.08 mm max height

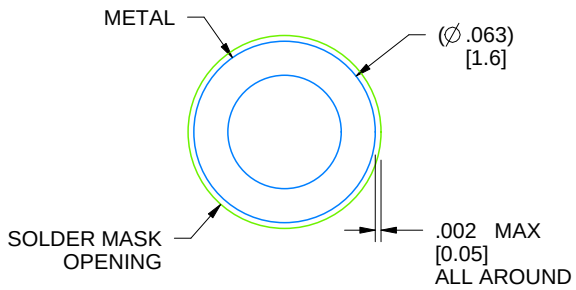
CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



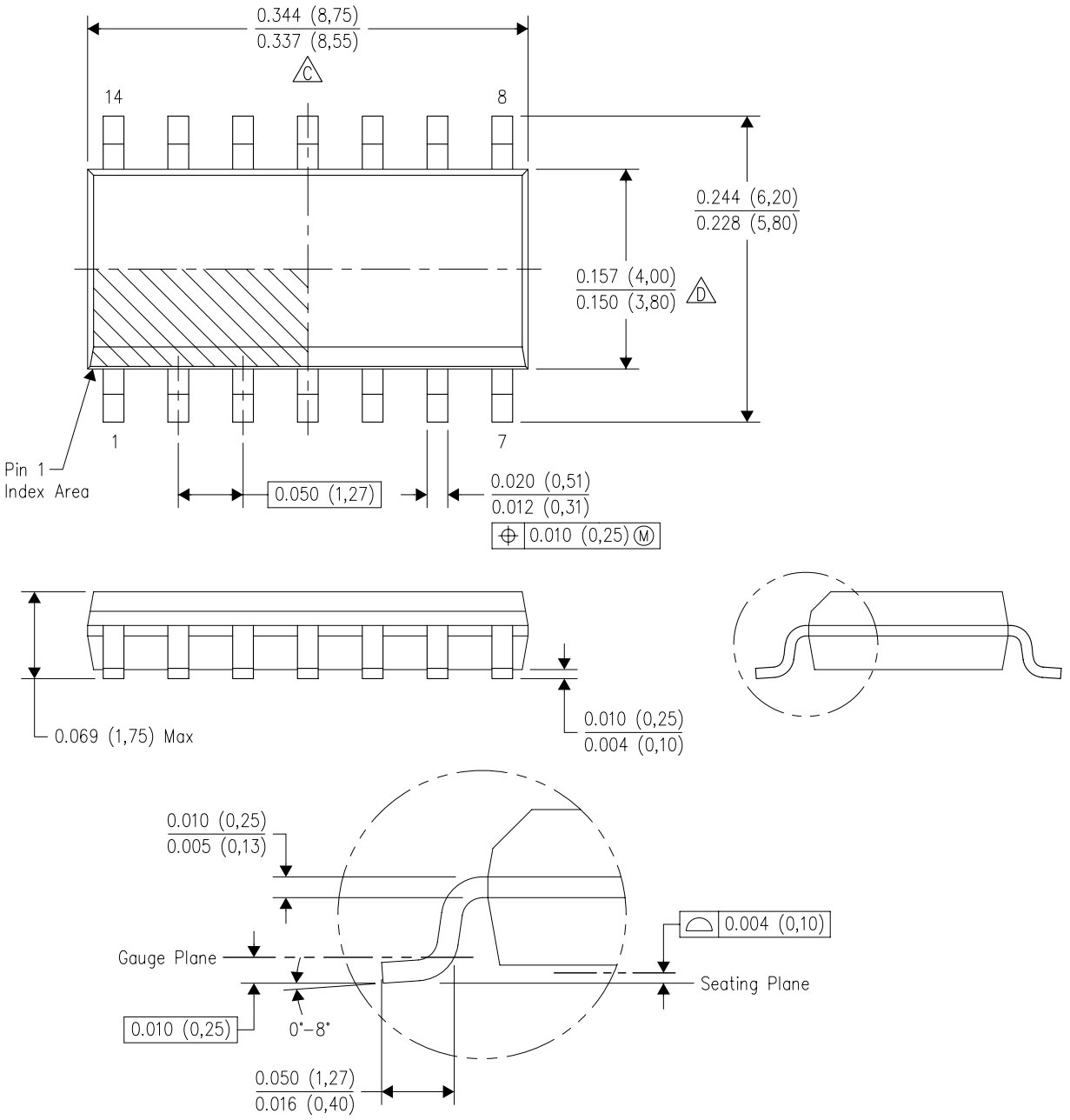
DETAIL A
SCALE: 15X



DETAIL B
13X, SCALE: 15X

4214771/A 05/2017

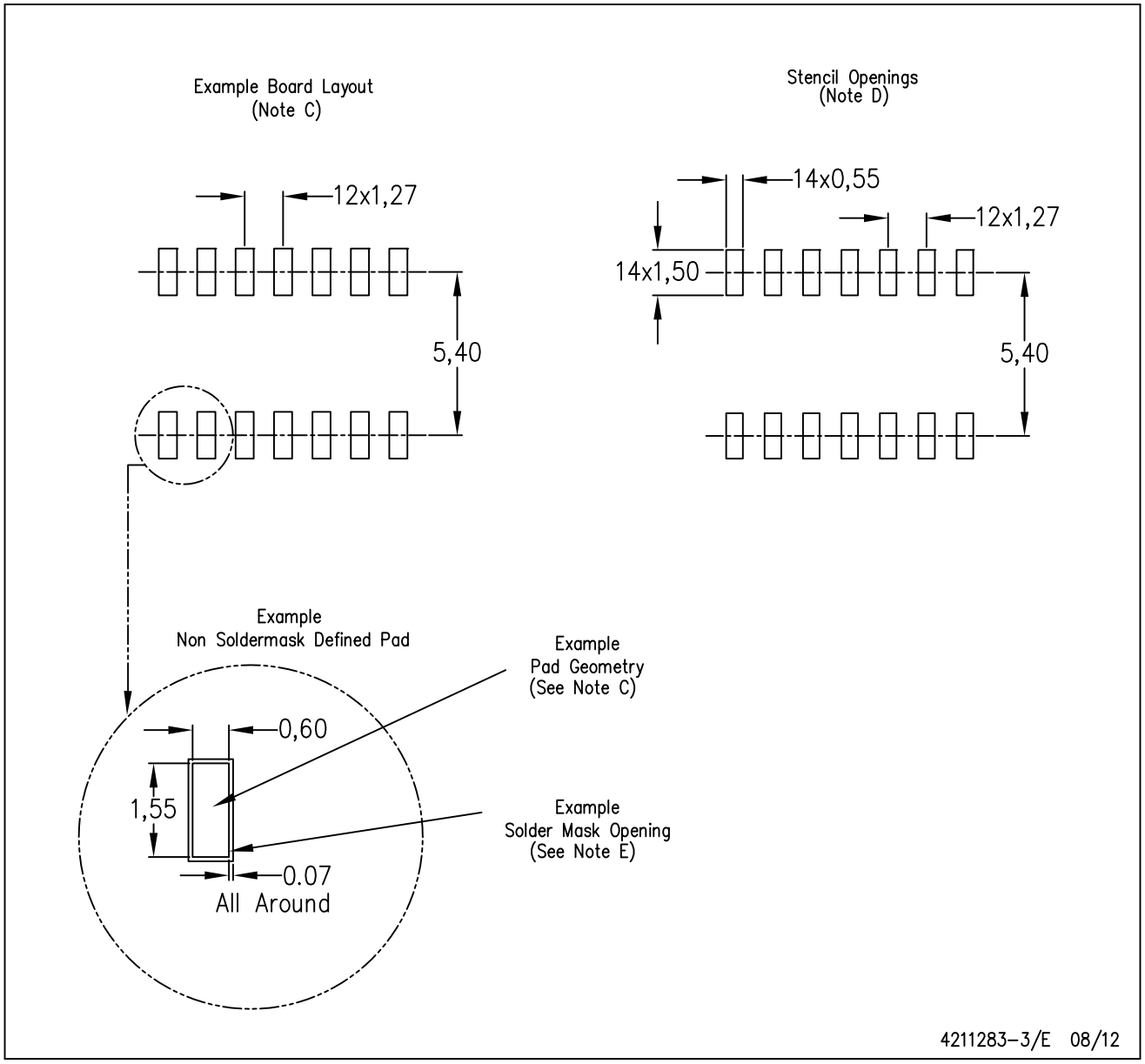
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2024, Texas Instruments Incorporated