



MOTOROLA

Pulse Width Modulation Control Circuit

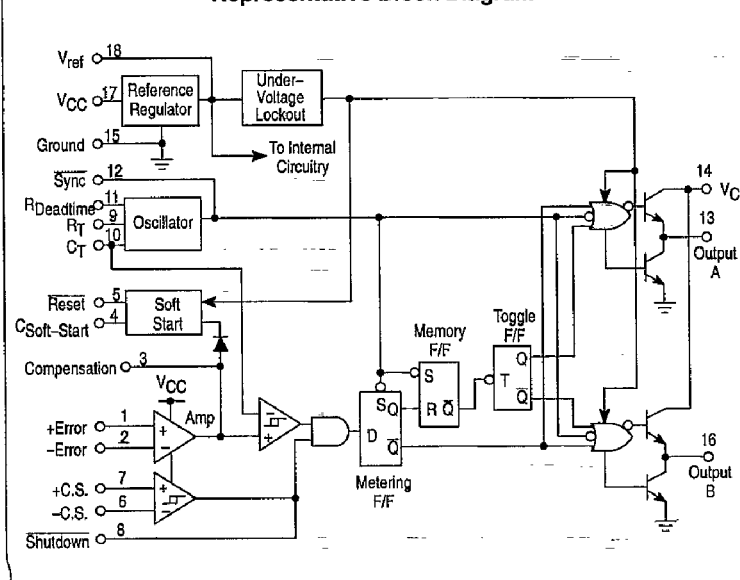
The SG3526 is a high performance pulse width modulator integrated circuit intended for fixed frequency switching regulators and other power control applications.

Functions included in this IC are a temperature compensated voltage reference, sawtooth oscillator, error amplifier, pulse width modulator, pulse metering and steering logic, and two high current totem pole outputs ideally suited for driving the capacitance of power FETs at high speeds.

Additional protective features include soft start and undervoltage lockout, digital current limiting, double pulse inhibit, adjustable dead time and a data latch for single pulse metering. All digital control ports are TTL and B-series CMOS compatible. Active low logic design allows easy wired-OR connections for maximum flexibility. The versatility of this device enables implementation in single-ended or push-pull switching regulators that are transformerless or transformer coupled. The SG3526 is specified over a junction temperature range of 0° to +125°C.

- 8.0 V to 35 V Operation
- 5.0 V $\pm 1\%$ Trimmed Reference
- 1.0 Hz to 400 kHz Oscillator Range
- Dual Source/Sink Current Outputs: ± 100 mA
- Digital Current Limiting
- Programmable Dead Time
- Undervoltage Lockout
- Single Pulse Metering
- Programmable Soft-Start
- Wide Current Limit Common Mode Range
- Guaranteed 6 Unit Synchronization

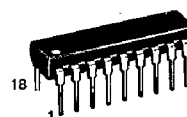
Representative Block Diagram



SG3526

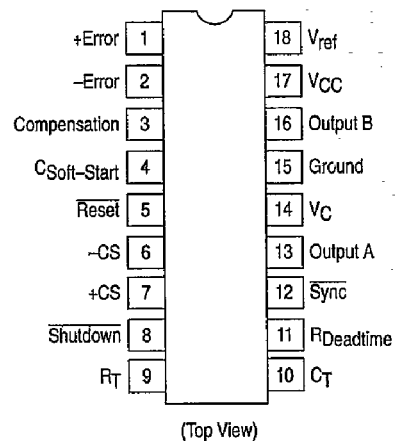
PULSE WIDTH MODULATION CONTROL CIRCUIT

SEMICONDUCTOR TECHNICAL DATA



N SUFFIX
PLASTIC PACKAGE
CASE 707

PIN CONNECTIONS



ORDERING INFORMATION

Device	Operating Temperature Range	Package
SG3526N	$T_J = 0^\circ \text{ to } +125^\circ \text{C}$	Plastic DIP

SG3526

MAXIMUM RATINGS (Note 1)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	+40	Vdc
Collector Supply Voltage	V_C	+40	Vdc
Logic Inputs		-0.3 to +5.5	V
Analog Inputs		-0.3 to V_{CC}	V
Output Current, Source or Sink	I_O	±200	mA
Reference Load Current ($V_{CC} = 40$ V, Note 2)	I_{ref}	50	mA
Logic Sink Current		15	mA
Power Dissipation $T_A = +25^\circ\text{C}$ (Note 3) $T_C = +25^\circ\text{C}$ (Note 4)	P_D	1000 3000	mW
Thermal Resistance Junction-to-Air	$R_{\theta JA}$	100	$^\circ\text{C/W}$
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	42	$^\circ\text{C/W}$
Operating Junction Temperature	T_J	+150	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$
Lead Temperature (Soldering, 10 Seconds)	T_{Solder}	±300	$^\circ\text{C}$

NOTES: 1. Values beyond which damage may occur.
2. Maximum junction temperature must be observed.
3. Derate at 10 mW/ $^\circ\text{C}$ for ambient temperatures above +50 $^\circ\text{C}$.
4. Derate at 24 mW/ $^\circ\text{C}$ for case temperatures above +25 $^\circ\text{C}$.

RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	8.0	35	Vdc
Collector Supply Voltage	V_C	4.5	35	Vdc
Output Sink/Source Current (Each Output)	I_O	0	±100	mA
Reference Load Current	I_{ref}	0	20	mA
Oscillator Frequency Range	f_{osc}	0.001	400	kHz
Oscillator Timing Resistor	R_T	2.0	150	k Ω
Oscillator Timing Capacitor	C_T	0.001	20	μF
Available Deadtime Range (40 kHz)	—	3.0	50	%
Operating Junction Temperature Range	T_J	0	+125	$^\circ\text{C}$

SG3526

ELECTRICAL CHARACTERISTICS ($V_{CC} = +15\text{ Vdc}$, $T_J = T_{low}$ to T_{high} [Note 5], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
REFERENCE SECTION (Note 6)					
Reference Output Voltage ($T_J = +25^\circ\text{C}$)	V_{ref}	4.90	5.00	5.10	V
Line Regulation ($+8.0\text{ V} \leq V_{CC} \leq +35\text{ V}$)	Reg_{line}	—	10	30	mV
Load Regulation ($0\text{ mA} \leq I_L \leq 20\text{ mA}$)	Reg_{load}	—	10	50	mV
Temperature Stability	$\Delta V_{ref}/\Delta T$	—	10	—	mV
Total Reference Output Voltage Variation ($+8.0\text{ V} \leq V_{CC} \leq +35\text{ V}$, $0\text{ mA} \leq I_L \leq 20\text{ mA}$)	ΔV_{ref}	4.85	5.00	5.15	V
Short Circuit Current ($V_{ref} = 0\text{ V}$) (Note 2)	I_{SC}	25	80	125	mA

UNDERVOLTAGE LOCKOUT

Reset Output Voltage ($V_{ref} = +3.8\text{ V}$)		—	0.2	0.4	V
Reset Output Voltage ($V_{ref} = +4.8\text{ V}$)		2.4	4.8	—	V

OSCILLATOR SECTION (Note 7)

Initial Accuracy ($T_J = +25^\circ\text{C}$)		—	± 3.0	± 8.0	%
Frequency Stability over Power Supply Range ($+8.0\text{ V} \leq V_{CC} \leq +35\text{ V}$)	$\frac{\Delta f_{osc}}{\Delta V_{CC}}$	—	0.5	1.0	%
Frequency Stability over Temperature ($\Delta T_J = T_{low}$ to T_{high})	$\frac{\Delta f_{osc}}{\Delta T_J}$	—	2.0	—	%
Minimum Frequency ($R_T = 150\text{ k}\Omega$, $C_T = 20\text{ }\mu\text{F}$)	f_{min}	—	0.5	—	Hz
Maximum Frequency ($R_T = 2.0\text{ k}\Omega$, $C_T = 0.001\text{ }\mu\text{F}$)	f_{max}	400	—	—	kHz
Sawtooth Peak Voltage ($V_{CC} = +35\text{ V}$)	$V_{osc(P)}$	—	3.0	3.5	V
Sawtooth Valley Voltage ($V_{CC} = +8.0\text{ V}$)	$V_{osc(V)}$	0.45	0.8	—	V

ERROR AMPLIFIER SECTION (Note 8)

Input Offset Voltage ($R_S \leq 2.0\text{ k}\Omega$)	V_{IO}	—	2.0	10	mV
Input Bias Current	I_{IB}	—	—350	—2000	nA
Input Offset Current	I_{IO}	—	35	200	nA
DC Open Loop Gain ($R_L \geq 10\text{ M}\Omega$)	A_{VOL}	60	72	—	dB
High Output Voltage ($V_{Pin\ 1} - V_{Pin\ 2} \geq +150\text{ mV}$, $I_{source} = 100\text{ }\mu\text{A}$)	V_{OH}	3.6	4.2	—	V
Low Output Voltage ($V_{Pin\ 2} - V_{Pin\ 1} \geq +150\text{ mV}$, $I_{sink} = 100\text{ }\mu\text{A}$)	V_{OL}	—	0.2	0.4	V
Common Mode Rejection Ratio ($R_S \leq 2.0\text{ k}\Omega$)	CMRR	70	94	—	dB
Power Supply Rejection Ratio ($+12\text{ V} \leq V_{CC} \leq +18\text{ V}$)	PSRR	66	80	—	dB

NOTES: 2. Maximum junction temperature must be observed.
 5. $T_{low} = 0^\circ\text{C}$ $T_{high} = +125^\circ\text{C}$
 6. $I_L = 0\text{ mA}$ unless otherwise noted.
 7. $f_{osc} = 40\text{ kHz}$ ($R_T = 4.12\text{ k}\Omega \pm 1\%$, $C_T = 0.01\text{ }\mu\text{F} \pm 1\%$, $R_D = 0\text{ }\Omega$)
 8. $0\text{ V} \leq V_{CM} \leq +5.2\text{ V}$.

ELECTRICAL CHARACTERISTICS (continued)

Characteristics	Symbol	Min	Typ	Max	Unit
PWM COMPARATOR SECTION (Note 7)					
Minimum Duty Cycle ($V_{\text{Compensation}} = +0.4 \text{ V}$)	DC_{min}	—	—	0	%
Maximum Duty Cycle ($V_{\text{Compensation}} = +3.6 \text{ V}$)	DC_{max}	45	49	—	%
DIGITAL PORTS (SYNC, SHUTDOWN, RESET)					
Output Voltage (High Logic Level) ($I_{\text{source}} = 40 \mu\text{A}$) (Low Logic Level) ($I_{\text{sink}} = 3.6 \text{ mA}$)	V_{OH} V_{OL}	2.4 —	4.0 0.2	— 0.4	V
Input Current — High Logic Level (High Logic Level) ($V_{\text{IH}} = +2.4 \text{ V}$) (Low Logic Level) ($V_{\text{IL}} = +0.4 \text{ V}$)	I_{IH} I_{IL}	— —	—125 —225	—200 —360	μA
CURRENT LIMIT COMPARATOR SECTION (Note 9)					
Sense Voltage ($R_{\text{S}} \leq 50 \Omega$)	V_{sense}	80	100	120	mA
Input Bias Current	I_{IB}	—	—3.0	—10	μA
SOFT-START SECTION					
Error Clamp Voltage ($\overline{\text{Reset}} = +0.4 \text{ V}$)		—	0.1	0.4	V
CSoft-Start Charging Current ($\overline{\text{Reset}} = +2.4 \text{ V}$)	I_{CS}	50	100	150	μA
OUTPUT DRIVERS (Each Output, $V_{\text{C}} = +15 \text{ Vdc}$, unless otherwise noted.)					
Output High Level $I_{\text{source}} = 20 \text{ mA}$ $I_{\text{source}} = 100 \text{ mA}$	V_{OH}	12.5 12	13.5 13	— —	V
Output Low Level $I_{\text{sink}} = 20 \text{ mA}$ $I_{\text{sink}} = 100 \text{ mA}$	V_{OL}	— —	0.2 1.2	0.3 2.0	V
Collector Leakage, $V_{\text{C}} = +40 \text{ V}$	$I_{\text{C(leak)}}$	—	50	150	μA
Rise Time ($C_{\text{L}} = 1000 \text{ pF}$)	t_{r}	—	0.3	0.6	μs
Fall Time ($C_{\text{L}} = 1000 \text{ pF}$)	t_{f}	—	0.1	0.2	μs
Supply Current (Shutdown = +0.4 V, $V_{\text{CC}} = +35 \text{ V}$, $R_{\text{T}} = 4.12 \text{ k}\Omega$)	I_{CC}	—	18	30	mA

NOTES: 7. $f_{\text{osc}} = 40 \text{ kHz}$ ($R_{\text{T}} = 4.12 \text{ k}\Omega \pm 1\%$, $C_{\text{T}} = 0.01 \mu\text{F} \pm 1\%$, $R_{\text{D}} = 0 \Omega$)
8. $0 \text{ V} \leq V_{\text{CM}} \leq +5.2 \text{ V}$
9. $0 \text{ V} \leq V_{\text{CM}} \leq +12 \text{ V}$

Figure 1. Reference Stability over Temperature

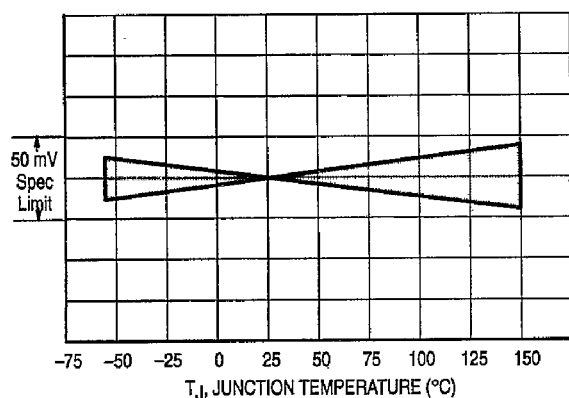


Figure 2. Reference Voltage as a Function Supply Voltage

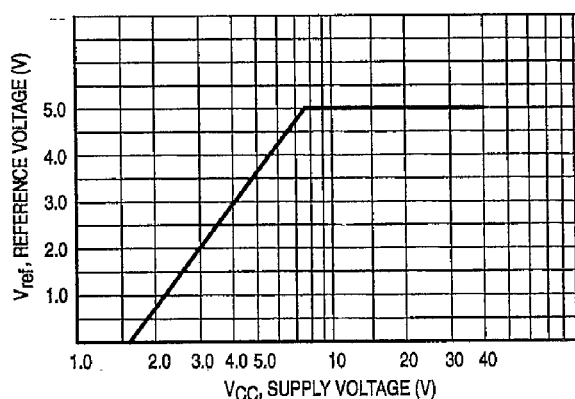


Figure 3. Error Amplifier Open Loop Frequency Response

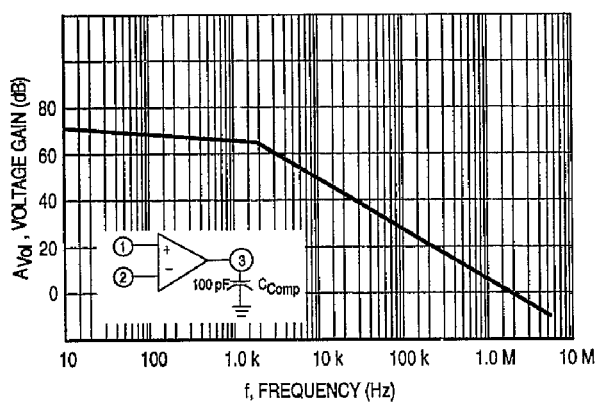


Figure 4. Current Limit Comparator Threshold

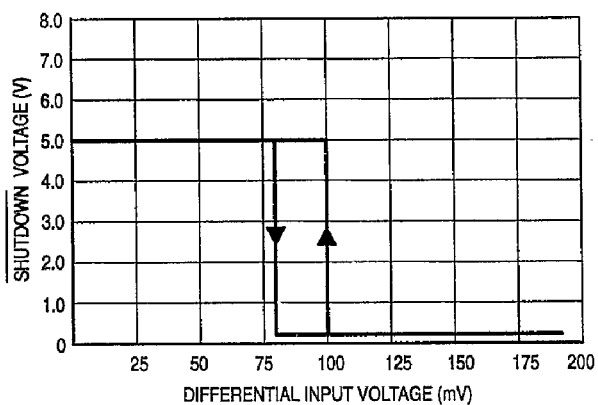


Figure 5. Undervoltage Lockout Characteristic

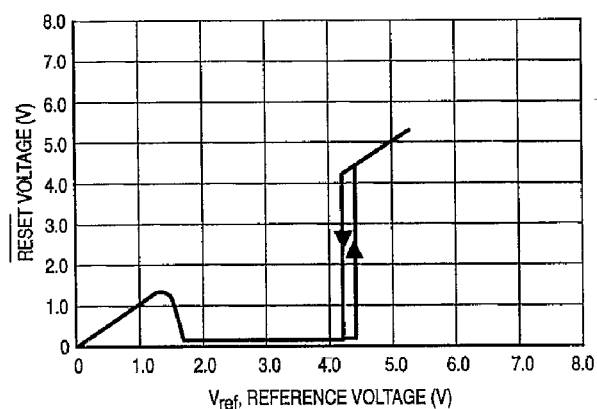


Figure 6. Output Driver Saturation Voltage as a Function of Sink Current

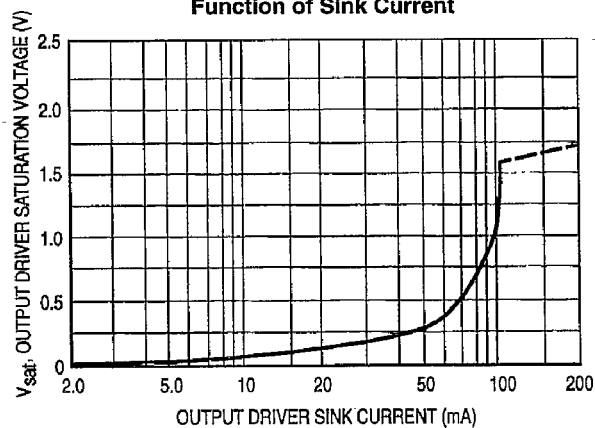


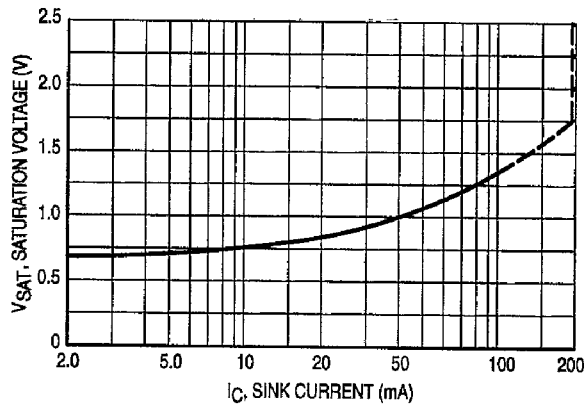
Figure 7. V_C Saturation Voltage as a Function of Sink Current

Figure 8. Oscillator Period

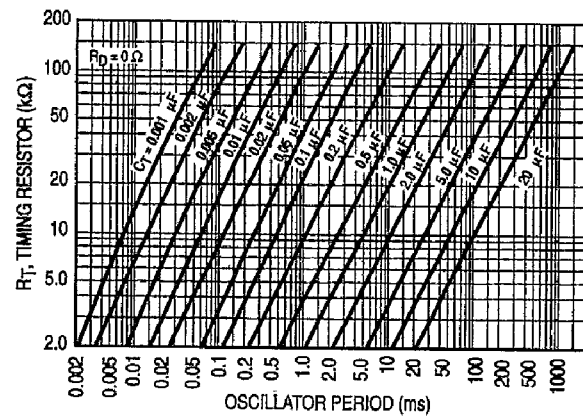


Figure 9. Error Amplifier

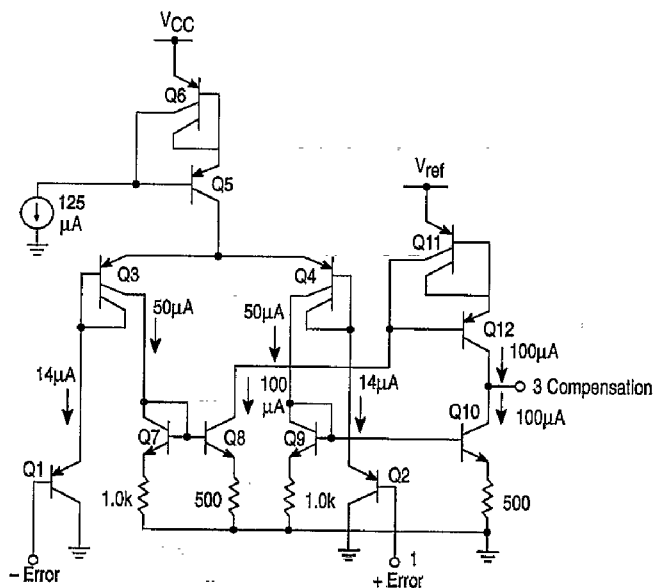


Figure 10. Undervoltage Lockout

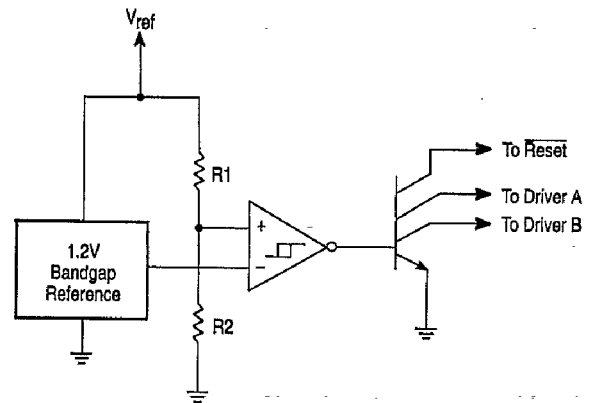
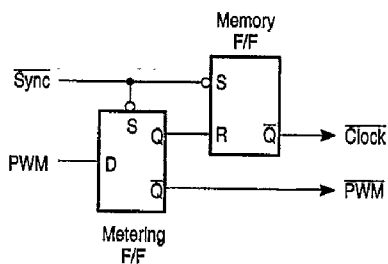


Figure 11. Pulse Processing Logic

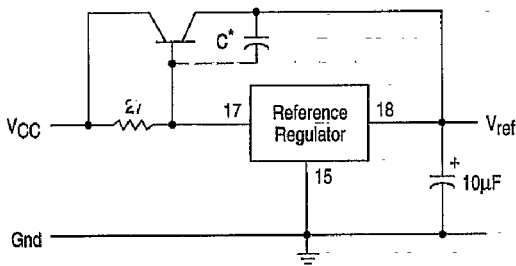


The metering Flip-Flop is an asynchronous data latch which suppresses high frequency oscillations by allowing only one PWM pulse per oscillator cycle.

The memory Flip-Flop prevents double pulsing in a push-pull configuration by remembering which output produced the last pulse.

APPLICATIONS INFORMATION

Figure 12. Extending Reference Output Current Capability



* May be required with some types of transistors

Figure 13. Error Amplifier Connections

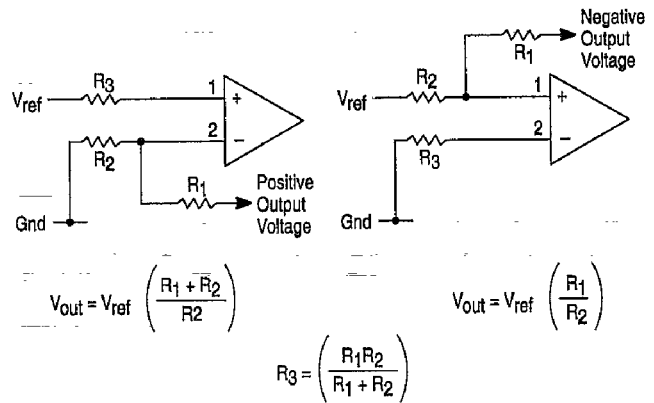


Figure 14. Oscillator Connections

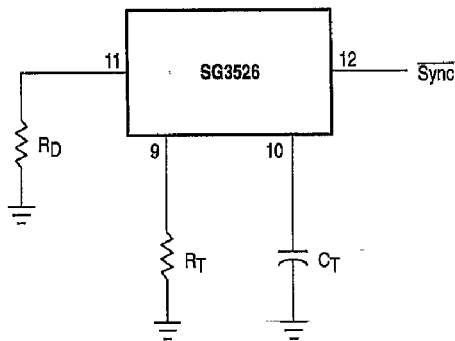


Figure 15. Foldback Current Limiting

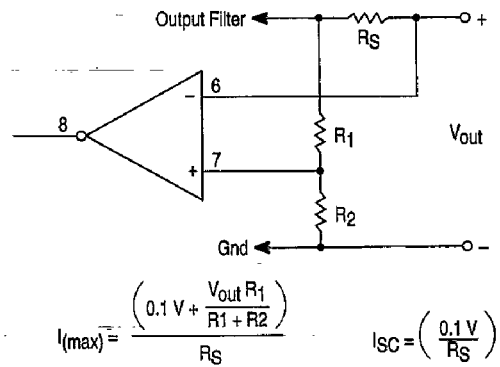


Figure 16. Soft-Start Circuitry

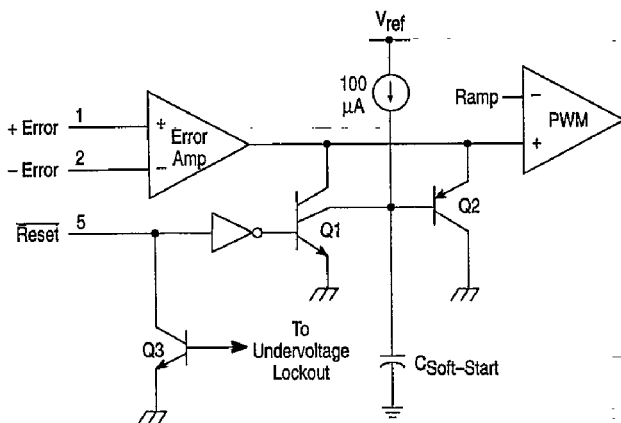
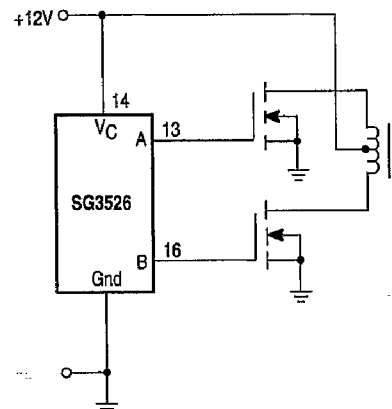


Figure 17. Driving VMOS Power FETs



The totem pole output drivers of the SG3526 are ideally suited for driving the input capacitance of power FETs at high speeds.

Figure 18. Half-Bridge Configuration

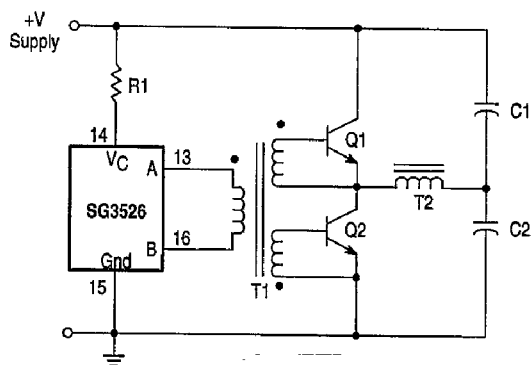
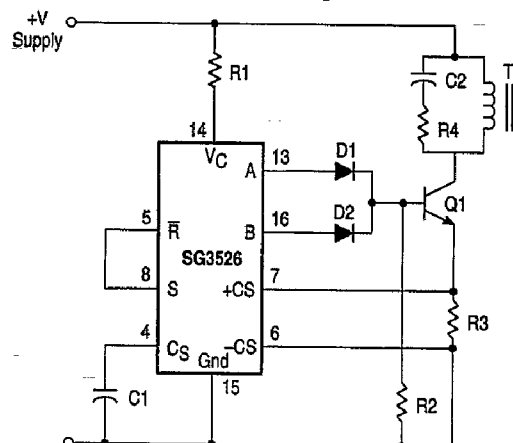


Figure 19. Flyback Converter with Current Limiting



In the above circuit, current limiting is accomplished by using the current limit comparator output to reset the soft-start capacitor.

Figure 20. Single-Ended Configuration

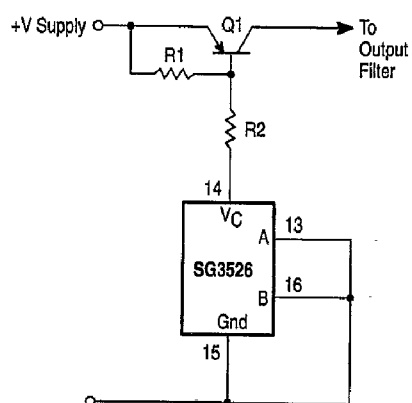


Figure 21. Push-Pull Configuration

